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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/659,832	09/11/2003	Dennis R. Esterberg	10006017-4	5946

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EXAMINER	
PEYTON, TAMMARA R	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 05/19/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/659,832	ESTERBERG ET AL.
	Examiner	Art Unit
	Tammara R Peyton	2182

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *11 September 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,5,8-11,13-17,19,20,22-24 and 26-29* is/are rejected.

7)☒ Claim(s) *2,3,6,7,12,18,21 and 25* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/11/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-29 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-33 (out of 58 total) of U.S. Patent No. 6,718,408. Although the conflicting claims are not identical, they are not patentably distinct from each other because both set of claims teach a computing device having one or more components each configured to perform a function in response to an input from an associated external device an input/output module configured for removable association with the computing device and having one or more input/output connectors configured to interface one or more associated external devices with the one or more components in the computing device; wherein the input/output module is

configured to pass one or more unmodified signals between the one or more components and the one or more associated external devices.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 4, 5, 8-11,13-17, 19, 20, 22-24, and 26-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over *Yanagisawa et al.,* (US 5,805,412).

1. As per claim 1, *Yanagisawa* teaches a system, comprising:

- a computing device (notebook computer, 100, Fig. 1) having one or more components (Fig.13) each configured to perform a function in response to an input from an associated external device (devices connected to the notebook computer's associated port(s));
- an input/output module (First docking unit, 200, Fig. 1, 4, 5 or combined First/Second docking unit, 300, Fig. 7) configured for removable association (Fig. 4) with the computing device and having one or more

input/output connectors (222, 231, 232, 233, 234, 235, 236, Fig.5 of First docking unit, 200) configured to interface one or more associated external devices (devices connected to the notebook computer's input/output connector port(s)) with the one or more components (notebook computer port signal lines, 25a, 25b, 25,c, 26a, 26b, 27a, 27b, Fig.13) in the computing device;

- wherein the input/output module (First docking unit, 200, Fig. 1, 4, 5, 13) is configured to pass one or more unmodified signals between the one or more components and the one or more associated external devices.

2. *Yanagisawa* does not expressly disclose wherein the input/output module (First docking unit, 200, Fig. 1, 4, 5, 13) is configured to pass one or more unmodified signals between the one or more components (Fig.13) and the one or more associated external devices. Nonetheless, the input/output connectors (shown in Fig. 13, 231-260e, 232-260g, 233-260h, 234-260h, 235-260i, 236-260j) each have dedicated signal lines represented as 260e-260j. Raw port signal(s) are generated from the input/output connectors (260e-260j) and transmitted to a signal line bundle, 260. The input/output module transmits the raw port signal (s) through signal line bundle, 260 to the notebook docking connector, 130. The raw port signal (s) are then branched to corresponding port signal lines (25a, 25b, 25,c, 26a, 26b, 27a, 27b, Fig.13). Referring to Fig. 13, Examiner is taking the position that the raw port signals generated from input/output connectors (shown in Fig. 13, 231-260e, 232-260g, 233-260h, 234-260h, 235-260i, 236-260j) are

simply passed through the input/output module to the notebook connector, 130 unmodified or not altered by the input/output module in any way. (Abstract, col. 5,lines 8-56, col. 8, lines 14-30, col. 13, lines 19-col. 14, lines 1-31)

3. As per claim 4, *Yanagisawa* teaches a system wherein:

- the input/output module (First docking unit, 200, Fig. 1, 4, 5/Second docking unit, Fig. 2) has multiple input/output connectors each configured to interface an external device with the computing device, wherein the input/output modules is configured to pass at least one input from an external device unmodified to a component in the computing device; and
- the input/output module has signal processing component to process an input from an external device, wherein the input/output module is configured to pass at least one processed input from the input/output module to the computing device.

4. *Yanagisawa* teaches a combined input/output module comprising of First docking unit, 200 and Second docking unit, 300. In one embodiment, the input/output module is comprises the First docking unit. In another embodiment, the input/output module comprises the First docking unit coupled to the Second docking unit. Signals received from the input/output connectors related to the First docking unit are passed to the notebook computer unmodified. However,

signals received from the input/output connectors related to the Second docking unit, specifically the signal from connector 324, are first processed and then passed to the notebook computer. A SCSI controller 364, performs protocol conversion on the received signal before passing the signal to the notebook computer. (col. 5, lines 47-col. 6, lines 1-26, 57-col. 7, lines 1-3, col. 15, lines 24-26)

5. As per claim 5, *Yanagisawa* teaches wherein the input/module comprising a parallel input/output connector and a serial input/output connector. Claim 5 is presented in alternative language requiring one "or" the other be found not necessarily all. Therefore, Examiner is taking the position that *Yanagisawa* teaches a input/output module comprising at least one or more of the listed connectors.

6. As per claims 9, *Yanagisawa* does not expressly teach of reserving system resources, nonetheless, a computer device configured to reserve system resources if a input/output connector does not have an associated external device connected is well known in the art, therefore, making use of the system obvious.

7. As per claim 10, it would have been obvious to one of ordinary skill that *Yanagisawa's* input/output module is configured to inform the computer device of

whether devices are connected to the input/output connector as it relates to the input/output connector configuration on the input/output module. (Fig.13)

8. As per claim 11, *Yanagisawa* teaches wherein the input/output module (First/Second docking unit, 300, Fig. 7) comprises a memory storage device (380, col. 14, lines 54-58) to store the related input/output connectors' configurations and informing the computing device of the configurations.

9. As per claim 13, *Yanagisawa* teaches wherein the input/output module does not expressly teach of de-allocating system resources, nonetheless, a computer device configured to reserve system resources if a input/output connector does not have an associated external device connected is well known in the art, therefore, making use of the system obvious.

10. As per claims 14 and 26, *Yanagisawa* teaches at least one interchangeable input/output module (First docking unit, 200/Second docking unit, 30) for a computer, comprising one or more input/output connectors supported by a module housing, each of which are configured to interface an external device with a component in the computer, at least one of the input/output connectors being configured to pass unmodified signals between its associated external device and its associated component. The First docking unit 200/Second docking unit 300 is interchangeable as it relates to changing the

structure of the notebook computer by attaching or detaching to and from the notebook computer. (see paragraph)

11. As per claim 15, *Yanagisawa* teaches wherein the module housing is configured to be removably attached to the computer.

12. As per claim 16, *Yanagisawa* another embodiment wherein the input/output module comprising of the First docking unit coupled to the Second docking unit. Signals received from the input/output connectors related to the First docking unit are passed to the notebook computer unmodified. However, signals received from the input/output connectors related to the Second docking unit, specifically the signal from connector 324, are first processed and then passed to the notebook computer. A SCSI controller 364, performs protocol conversion on the received signal before passing the signal to the notebook computer. (col. 5, lines 47-col. 6, lines 1-26, 57-col. 7, lines 1-3, col. 15, lines 24-26)

13. As per clam 17, *Yanagisawa* teaches wherein the input/module comprising a parallel input/output connector and a serial input/output connector.

14. As per claim 19 and 28, it would have been obvious to one of ordinary skill that *Yanagisawa's* input/output module is configured to inform the computer device of whether devices are connected to the input/output connector as it

relates to the input/output connector configuration on the input/output module. (Fig.13)

15. As per claim 20, *Yanagisawa* teaches wherein the input/output module (First/Second docking unit, 300, Fig. 7) comprises a memory storage device (380, col. 14, lines 54-58) to store the related input/output connectors' configurations and informing the computing device of the configurations.

16. As per claims 22 and 23, *Yanagisawa* teaches a method, comprising:

- providing an input/output module (First docking unit, 200, Fig. 1, 4, 5 or combined First/Second docking unit, 300, Fig. 7) configured for removable attachment to a computer that contains multiple components that can interface with different external devices (connected to the notebook computer's input/output connector port(s)); and
- providing multiple different input/output connectors supported by the input/output module, at least some of the input/output connectors (222, 231, 232, 233, 234, 235, 236, Fig.5 of First docking unit, 200) being configured to establish a connection between an external device and an associated component in the computer (notebook computer, 100, Fig. 1) and pass signals in an unmodified form between the external device and its associated component. (notebook computer port signal lines, 25a, 25b, 25,c, 26a, 26b, 27a, 27b, Fig.13, see Abstract, col. 5,lines 8-56, col. 8, lines 14-30, col. 13, lines 19-col. 14, lines 1-31)

17. As per clam 24, *Yanagisawa* teaches wherein the input/module comprising a parallel input/output connector and a serial input/output connector.

18. As per claim 27, *Yanagisawa* a method further comprising:

of receiving a second input from a second external device (connected to one of the connectors) with a second input/output connector (324, Fig.14) on the interchangeable input/output module;

processing the second input with a signal processing component in the interchangeable input/output module to form a processed input;

passing the processed input from the signal processing component in the input/output module to a component in the computing device. (col. 5, lines 47-col. 6, lines 1-26, 57-col. 7, lines 1-3, col. 15, lines 24-26)

19. As per claim 28, *Yanagisawa* does not expressly teach of reserving system resources, nonetheless, a computer device configured to reserve system resources if a input/output connector does not have an associated external device connected is well known in the art, therefore, making use of the system obvious.

Allowable Subject Matter

Claims 2, 3, 6, 7, 12, 18, 21, and 25 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tammara Peyton whose telephone number is (703) 306-5508. The examiner can normally be reached between 6:30 - 4:00 from Monday to Thursday, (I am off every first Friday), and 6:30-3:00 every second Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jeffrey A. Gaffin, can be reached on (703) 308-3301. The fax phone number for the organization where this application or proceeding is assigned is (703) 305-3718. Any inquiry of a general nature of relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Mailed responses to this action should be sent to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231.

Faxes for Official/formal (After Final) communications or for informal or draft communications (please label "PROPOSED" or "DRAFT") sent to:

(703) 872-9306

Hand-delivered responses should be brought to:

USTPO, 2011 South Clark Place, Customer Window

Crystal Plaza Two, Lobby Room 1B03, Arlington, VA, 22202Crystal Park II, 2121.

Tammara Peyton

May 15, 2004